HIT 2 010-1-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

N. MITSUISHI

Serial No. 09/240,975 Group Art Unit: 2188

Filed: January 29, 1999 Examiner: R. Bragdon

For: AN IC CARD HAVING A DEDICATED WRITE CONTROLLER FOR WRITING TO INCORPORATED EEPROM ON THE CARD (As Amended)

APPEAL BRIEF

Assistant Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This appeal is taken from the final rejection of claims 31-34 as set forth in the Office Action of December 4, 2003. In accordance with 37 CFR § 1.192, Appellants address the following items.

REAL PARTY IN INTEREST

The real party in interest is Hitachi, Ltd. of Tokyo, Japan.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 31-34 are pending and have been finally rejected, accordingly, the rejection of these claims is on appeal.

STATUS OF AMENDMENTS

Appellants have not filed any Amendments after the final Office Action.

SUMMARY OF THE INVENTION

An embodiment of the overall construction of microcomputer 10 is shown in Figs. 1 and 2. A RAM 2 provides the work memory of CPU 1. I/O Unit 5 is provided for the exchange of data (Dx) to and from the outside of the micrcomputer. Fig. 2 also shows a peripheral circuit 6, an EEPROM 4 that stores a program and data and a write control unit 7. *See*, page 6, lines 21 of the specification. The flow of data Dx in the microcomputer of Fig. 2 is shown in Fig. 3. A user program region M1 and a data region M2 are preferably disposed in EEPROM 4, as shown in Fig. 4, for example.

Fig. 1 shows a switch that illustratively denotes that the program controlling execution of the CPU 1 is transferred to mask ROM 3 and then returned to a program in EEPROM 4 by return instruction after completion of a write operation.

Fig. 5 also shows, in step S5, that after completion of the write operation the CPU is returned to the user program region of the EEPROM 4 to read the user program and execute the user program's normal operation. Accordingly, the CPU becomes a write controller for writing program and data to EEPROM 4.

With respect to the invention as claimed, a write operation is disclosed wherein the CPU 1 receives a program (first program) from outside the microcomputer through the I/O unit 5 in accordance with the program (second program) stored in mask ROM 3. In this way, a first program and data to be stored in the EEPROM is supplied from outside of the semiconductor chip via the input and output circuit. The write operation is performed by the CPU executing the write control program (second program). That is, the write operation directly writes to the user program region M1 of EEPROM 4 from an exterior data source that is in communication with the CPU. *See*, page 9, lines 30-35 of the specification.

According to the invention, since the CPU 1 receives the program through I/O unit 5 in accordance with execution of a write control program stored in the memory of mask ROM 3, direct access to the EEPROM 4 from outside is prevented to

maintain secrecy. *See*, page 9, last line to page 10, line 6 of the specification.

With respect to the invention set forth in claim 33, see page 14, lines 1-5 from the bottom of the page. An example is set forth of the write control program being stored in advance in mask ROM 3 and when the write operation to EEPROM 4 is made, the write control program is transferred to RAM 2 in order to let the CPU 1 execute the write control program from the RAM.

ISSUES ON APPEAL

The sole issue on appeal is the propriety of the rejection of claims 31-34 under 35 U.S.C. § 103 as being unpatentable over Ugon, U.S. Patent No. 4,382,279 in view of Goss et al. ("Single Chip Microcomputer with EPROM Allows Flexible System Design").

GROUPING OF CLAIMS

Each of pending claims 31-34 is separately patentable.

ARGUMENT

References Relied Upon by the Examiner

1. Ugon, U.S. Patent No. 4,382,279

2. Goss et al. (Goss), "Single Chip Microcomputer with EPROM Allows Flexible System Design", Electronic Design, March 3, 1983.

Discussion of the Differences Between the Claimed Invention and the Applied References

According to the present invention, as set forth in claims 31-34, a microcomputer on a semiconductor chip includes an electrically erasable and programmable ROM (hereinafter EEPROM) capable of storing a program and data. The program to be stored in the EEPROM is a first program, such as a user program, that includes an instruction which changes a process of the central processing unit to a process that controls writing of the EEPROM based on the second program, such as a write control program, stored in a memory, such as mask ROM 3.

The first program, which may be a user program, and data to be stored in the EEPROM is supplied from outside of the semiconductor chip via the input and output circuit. Further,

the first program and data are written into the EEPROM by the central processing unit executing the write control program. That is, the central processing unit controls the write control circuit based on the execution of the write control program. According to the present invention, the first program may be an operation program that can be changed by the CPU executing the write control program. Thus, if a program bug is found in the program that has been stored in the EEPROM, a revised new program can be programmed into the EEPROM after erasing the program having the bug in it.

Accordingly, the claimed microcomputer on a semiconductor chip may, for example, be a microprocessor with flash memory. In such a case, the flash memory can store the operation program and the data that is supplied from the outside of the microprocessor and the operation program can be programmed into the flash memory by setting an operation mode of the microprocessor into a predetermined programming mode, e.g. a PROM writer programming mode or on-board programming mode. If a program bug is found in the operation program stored in the flash memory or a new operation program is developed, the reprogramming of the flash memory can be performed.

In Ugon, the disclosed microprocessor architecture includes an EPROM 101, which is relied upon in the Office Action for including a write control circuit that is equivalent to that of the present invention. However, the microcomputer of the invention, which includes the claimed write control circuit and the EEPROM of the invention are not disclosed or rendered obvious by the disclosure of Ugon.

Specifically, Ugon discloses that:

> In the majority of applications it is possible to construct the program in such a way that memory block M1 contains all the non-evolving programs or parts of programs and block M2 contains the evolving programs or parts of programs. In an application of this kind memory block M1 can be produced in the form of a read-only memory (ROM) to reduce manufacturing costs and the physical area of this part of the memory; in this case there is no longer a write voltage V.sub.p1. The second memory block M2 on the other hand must necessarily be in the form of a PROM or EPROM memory (emphasis added). (See col. 6, lines 1-15 of the reference.)

Further, col. 6, lines 55 to 68 of the Ugon reference discloses that:

> With this architecture, a program which is executed in blocks M1 and M2 of memory 101 modifies the information content of memory block M2. More particularly, if the program is to modify the memory content at an address 2FOH (i.e., the 752nd word in the memory) using the result of an operation situated in the accumulator 108, the program stores the address 2FOH beforehand in the working registers

> R0 and R1 of the set 111.
>
> The automatic programming is performed by a sub-program called "PROG" which is stored in memory block M1. This sub-program PROG needs to perform all the functions required for writing in the memory 101 and, in particular, needs to use sequences which are compatible with the fabrication technology employed (emphasis added).

That is, in Ugon, memory Block M1 contains all the non-evolving part of the programs, and memory block M2 contains the evolving part of the programs. The content of memory block M2 is modified by the program that is executed in blocks M1 and M2 of memory 101. Accordingly, one having ordinary skill in the art would consider that the non-evolving part of the program corresponds to an operation program or a data processing program, and the evolving part of the programs corresponds to data that is used by the operation program or data processing program. Accordingly, in the Ugon reference, the non-evolving part of the program in memory block M1 is not clearly disclosed as being modified.

On the other hand, in the present invention, as defined by claim 31, an EEPROM is claimed that is capable of storing a first program and data, and the central processing unit performs a writing to the EEPROM of the first program and data from outside of the semiconductor chip via the input and

output unit. The writing is performed by controlling a write control circuit based on the second program (write control program) stored in the memory. Further, according to claim 31, the EEPROM is claimed as being capable of storing a first program and data, wherein significant amounts of the first program are written in a write process where the CPU controls the write control circuit by executing the second program, such as the write control program that is stored in the memory (mask ROM according to claim 32).

In Ugon, there is no disclosure suggesting that the memory block M2 stores a program, such as an operation program, in which significant amounts of the program are written to the memory block (M2) from outside the semiconductor chip in a manner comparable to that of the present invention. The Examiner recognizes that the disclosure of Ugon is limited because the reference does not disclose that significant amounts of a program, such as an operation program, are written to the memory block (M2) from outside the semiconductor chip in a write process where the CPU controls a write control circuit by executing a write

control program. Accordingly, Goss is applied in combination with Ugon.

Goss is relied upon for disclosing a microcomputer with an EEPROM that can be reprogrammed by downloading data to the processor. However, the combination of Goss and Ugon does not render the invention set forth in claims 31-34 obvious under 35 U.S.C. § 103(a) for the following reasons.

The claimed invention of claim 31 is not obvious merely because Goss discloses the reprogramming of an EEPROM of a microcomputer from outside the chip. The Office Action does not identify any disclosure in Ugon or Goss that provides the suggestion to modify the PROG (subroutine) stored in memory M1 of Ugon to include writing significant amounts of an operation program stored in an EPROM from outside the chip. Further, neither reference suggests or teaches replacing the memory M1 of Ugon with RAM, so that the RAM could then receive a copy of the subroutine PROG, as stated in the Office Action. Rather, the suggestions set forth in the Office Action that it would be obvious to one of ordinary skill in the art to make the modifications to Ugon as proposed result from impermissible hindsight reconstruction of the invention from the references.

Although reconstruction of the prior art in support of an obviousness rejection is permitted, the Examiner is not at liberty to pick and choose elements form the prior art to make combinations that are not suggested by the references themselves. Goss merely discloses an EEPROM that is designed to be more versatile than a mask ROM. Goss states that "Previous microcomputers with their fixed mask programmed ROM programs had to be replaced manually whenever there was a demand for updating ..." (*see* page 1 of the article, left col., lines 12-17). Accordingly, the EEPROM of Goss has the advantage of being programmable, unlike mask ROMs, and therefore the teaching of the reference to one having ordinary skill in the art is rather narrow, and concerns the reprogramming of the EEPROM. Therefore, the combination of Ugon and Goss does not suggest the invention as claimed in claim 31, which includes the first and second programs, and in which the second program is a write control program that when executed controls the write control circuit to perform a writing to the EEPROM of significant amounts of the first program.

With respect to claim 32, the microcomputer of the invention includes an EEPROM and in addition a mask ROM as the memory that stores the write control program, which is not disclosed or suggested by the combination of Ugon and Goss. Accordingly, in addition to the arguments presented above with respect to the patentability of claim 31, claim 32 is separately patentable over the Ugon and Goss combination.

In addition to the arguments presented above with respect to the patentability of claims 31 and 32, claim 33 is separately patentable over the Ugon and Goss combination for adding to the claimed combination that the memory which stores the write control program is a RAM that receives the write control program from the mask ROM. Accordingly, the combination claimed in claim 33, which includes the mask ROM and a RAM in addition to the EEPROM is not fairly suggested by the combination of Ugon and Goss.

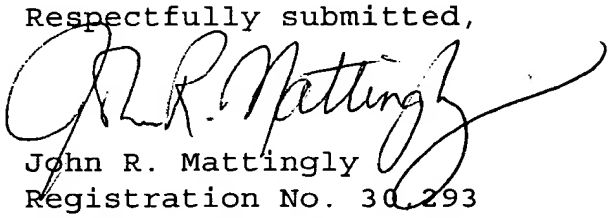
In addition to the arguments presented above with respect to the patentability of claim 31, claim 34 is separately patentable over the Ugon and Goss combination for adding to the claimed combination the data bus to which the central processing unit, the input and output unit, the ROM and the

memory are coupled, and further the address bus to which the central processing unit, the input and output unit, the electrically programmable ROM and the memory are coupled.

CONCLUSION

The final rejection of the Examiner rejecting claims 31-34 as being unpatentable over Ugon and Goss under 35 U.S.C. § 103 should be reversed.

Respectfully submitted,



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CLAIM ON APPEAL

31. A microcomputer on a semiconductor chip, the microcomputer comprising:

a central processing unit;

an electrically erasable and programmable ROM capable of storing a first program as an operation program of the central processing unit and data;

a write control circuit which performs a writing of the first program or the data to the ROM under control of the central processing unit;

a memory in which a second program as a write control program for writing to the ROM is stored; and

an input and output unit;

wherein the central processing unit performs a writing to the ROM of the first program input from outside of the semiconductor chip via the input and output unit by controlling the write control circuit based on the second program,

wherein the first program includes an instruction which changes a process of the central processing unit to a process that controls a writing of the ROM based on the second program stored in the memory,

wherein the second program includes an instruction which returns the process of the CPU to a process based on the first program stored in the ROM after completion of the process that controls the writing of the ROM, and

wherein significant amounts of the first program stored in the ROM are written in a write process where the central processing unit controls the write control circuit by executing the second program.

32. A microcomputer according the claim 31,

wherein the memory which stores the write control program is a mask ROM.

33. A microcomputer according to claim 32,

wherein the memory which stores the write control program is a RAM that receives the write control program from the ROM.

34. A microcomputer according to claim 31, further comprising:

a data bus to which the central processing unit, the input and output unit, the ROM and the memory are coupled; and

an address bus to which the central processing unit, the input and output unit, the electrically programmable ROM and the memory are coupled.